Docket No. 00884.229US1 Client Ref. No. P7912

**Clean Version of Pending Claims**

DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION
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Serial No.: 09/460,742



4. [Twice Amended] A circuit comprising:

a voltage node;

a ground node; and

a transistor including a gate, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node, the transistor operating in the depletion mode, the gate comprising a p-type polysilicon, wherein the transistor has a variable capacitance characteristic that is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value.

5. The circuit of claim 4, wherein the operating voltage value is between about .5 volts and about 1.5 volts.

6. The circuit of claim 5, further comprising:

a logic cell coupled to the voltage node and located in close proximity to the transistor.

9. A circuit comprising:

a die having a high power supply voltage node and a low power supply voltage node; and

a transistor coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

10. The circuit of claim 9, wherein the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and the drain are coupled to the low power supply voltage node.

14. [Twice Amended] A circuit comprising:

a die;

a ground node located on the die;

a power supply voltage node located on the die; and

an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node.

15. The circuit of claim 14, wherein incremental voltage variations of one polarity are damped and incremental voltage variations of the opposite polarity are amplified.

16. The circuit of claim 14, wherein the operational node voltage is about 1.3 volts.